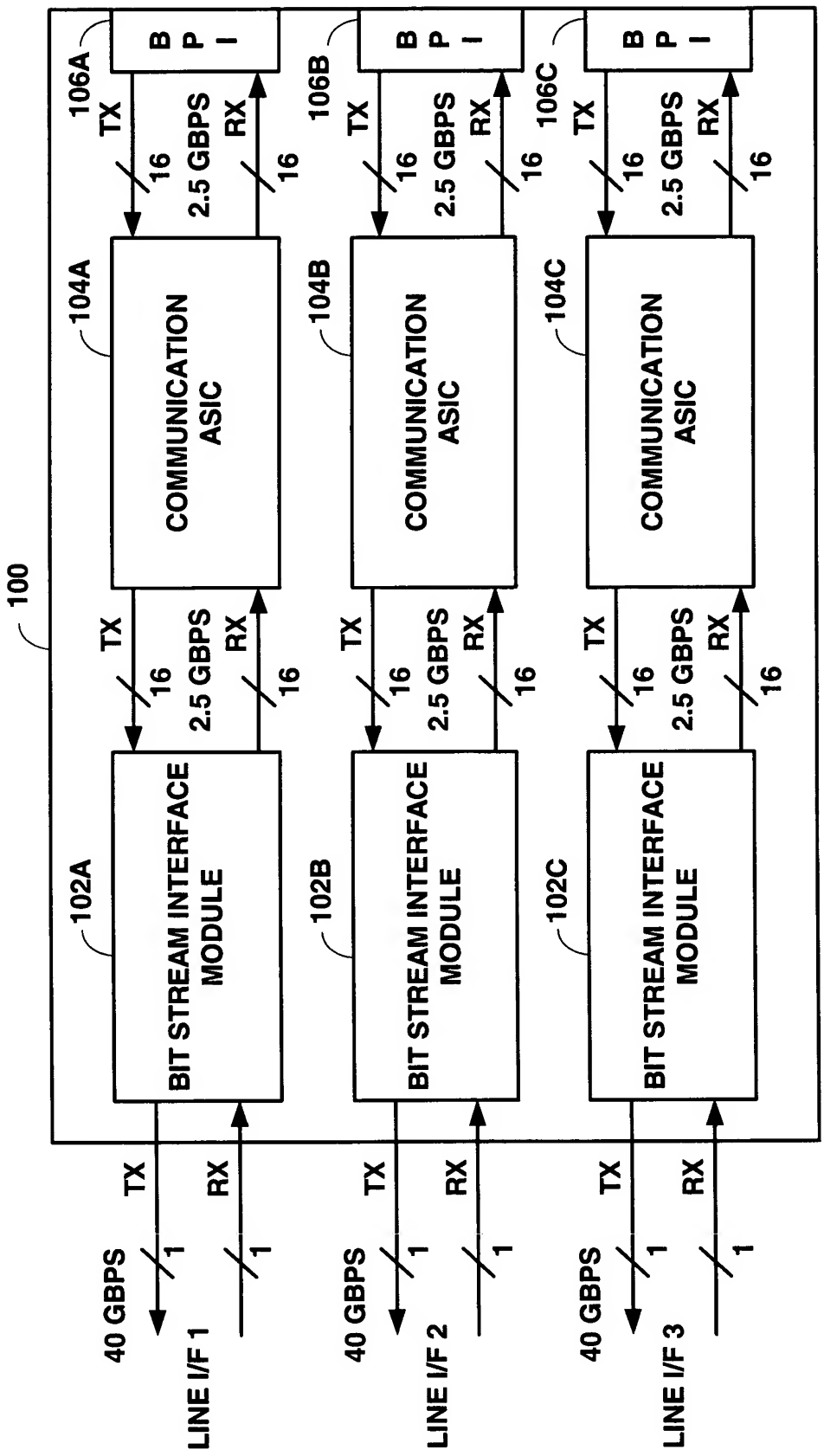

100
102A
BIT STREAM INTERFACE MODULE
102B
BIT STREAM INTERFACE MODULE
102C
BIT STREAM INTERFACE MODULE
104A
COMMUNICATION ASIC
104B
COMMUNICATION ASIC
104C
COMMUNICATION ASIC
106A
B P I
106B
B P I
106C
B P I
TX
RX
16
2.5 GBPS
40 GBPS
1
LINE I/F 1
LINE I/F 2
LINE I/F 3

FIG. 1

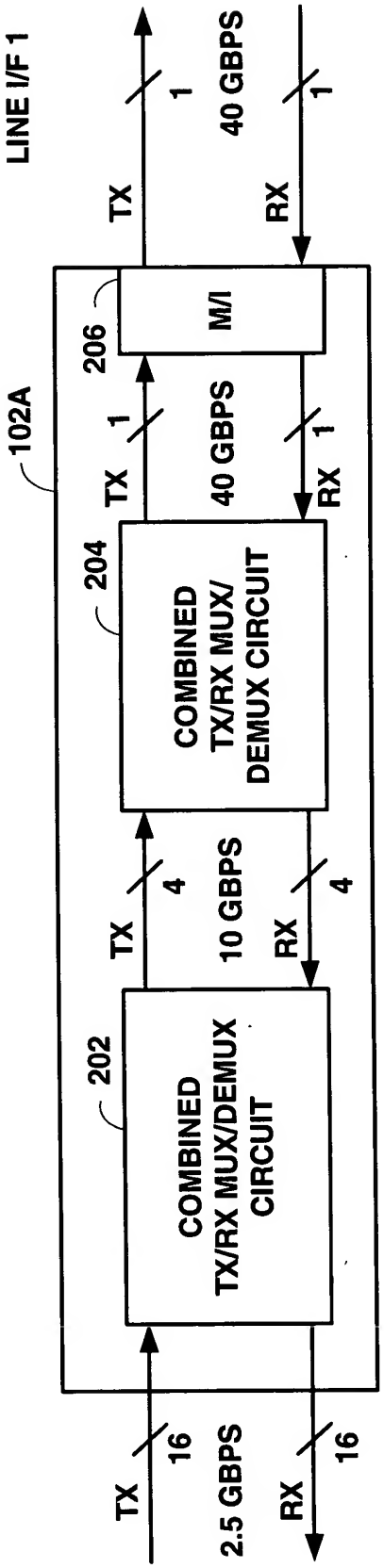

LINE I/F 1
102A
TX
16
2.5 GBPS
RX
16
202
COMBINED TX/RX MUX/DEMUX CIRCUIT
TX
4
10 GBPS
RX
4
204
COMBINED TX/RX MUX/ DEMUX CIRCUIT
TX
1
40 GBPS
RX
1
206
M/I
TX
1
40 GBPS
RX
1

FIG. 2A

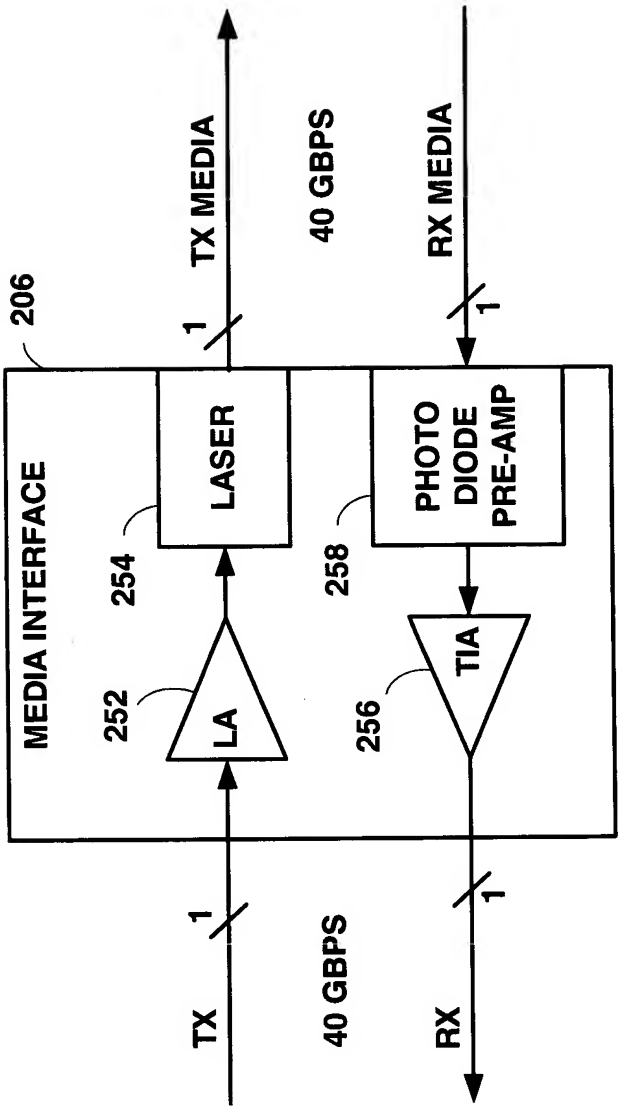

206
MEDIA INTERFACE
252
LA
254
LASER
256
TIA
258
PHOTO DIODE PRE-AMP
TX
1
40 GBPS
RX
1
TX MEDIA
1
40 GBPS
RX MEDIA
1

FIG. 2B

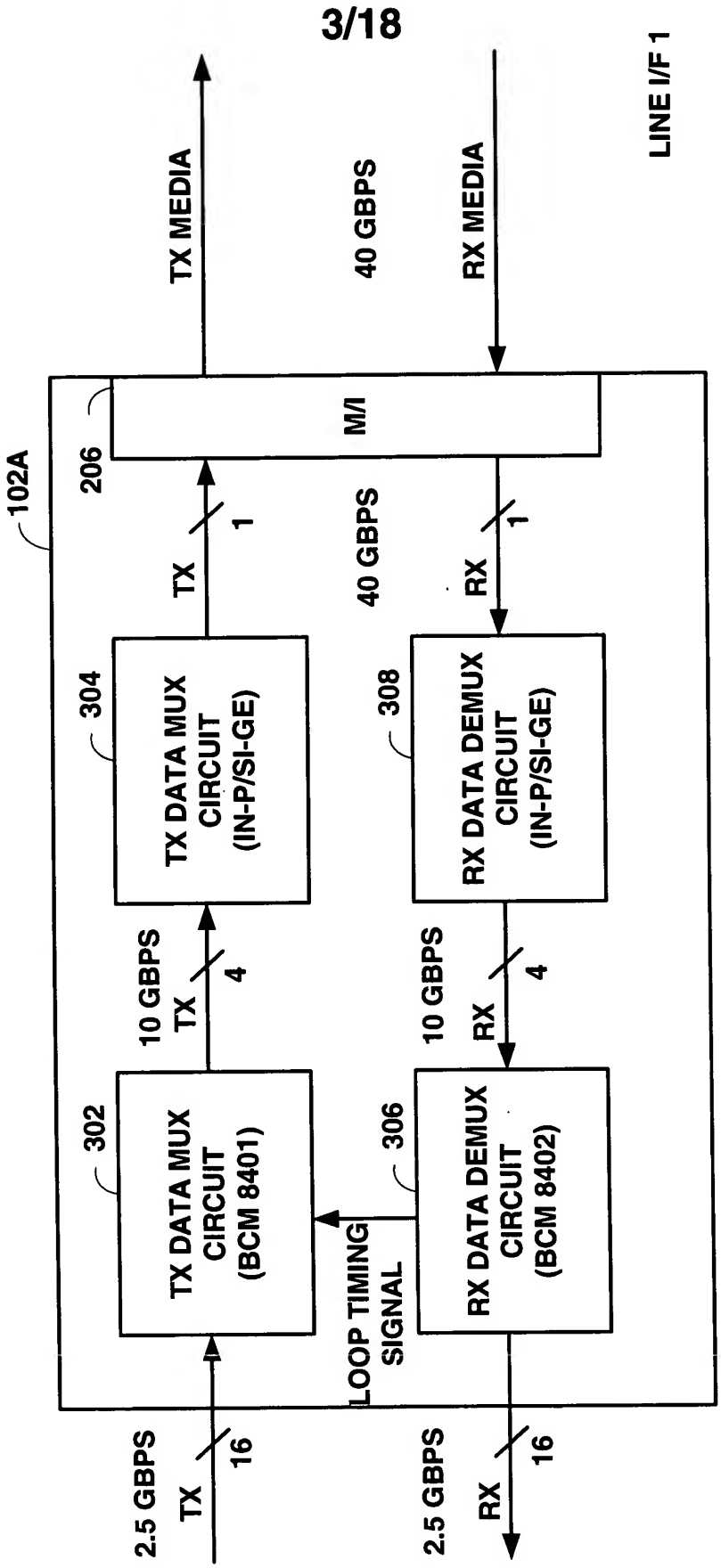

LINE I/F 1
TX MEDIA
40 GBPS
RX MEDIA
102A
206
M/I
TX
1
40 GBPS
RX
1
304
TX DATA MUX CIRCUIT (IN-P/SI-GE)
308
RX DATA DEMUX CIRCUIT (IN-P/SI-GE)
10 GBPS
TX
4
10 GBPS
RX
4
302
TX DATA MUX CIRCUIT (BCM 8401)
306
RX DATA DEMUX CIRCUIT (BCM 8402)
LOOP TIMING SIGNAL
2.5 GBPS
TX
16
2.5 GBPS
RX
16

FIG. 3

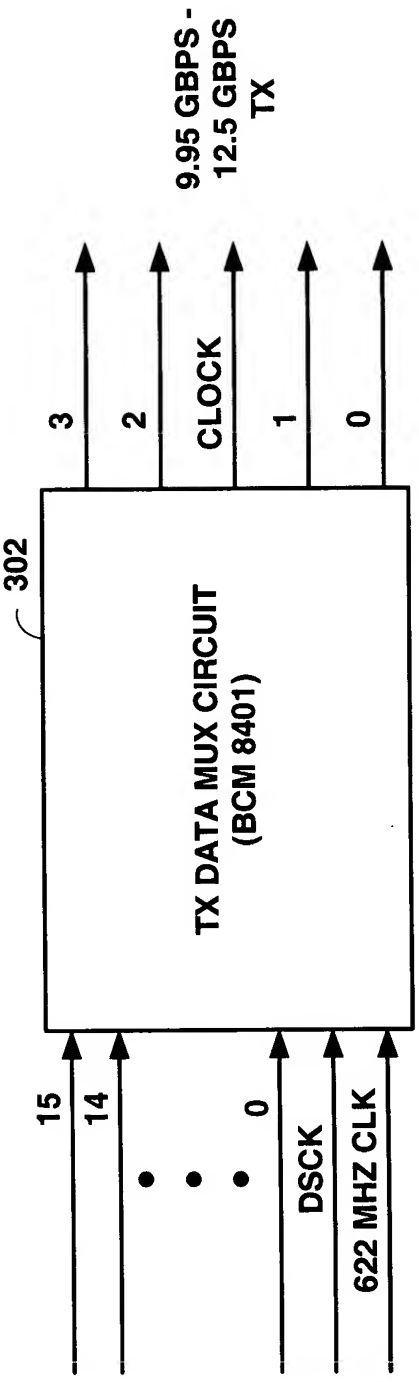

302
TX DATA MUX CIRCUIT
(BCM 8401)
15
14
0
DSCK
622 MHZ CLK
2.5 GBPS - 3.125 GBPS TX
3
2
CLOCK
1
0
9.95 GBPS - 12.5 GBPS TX

FIG. 4A

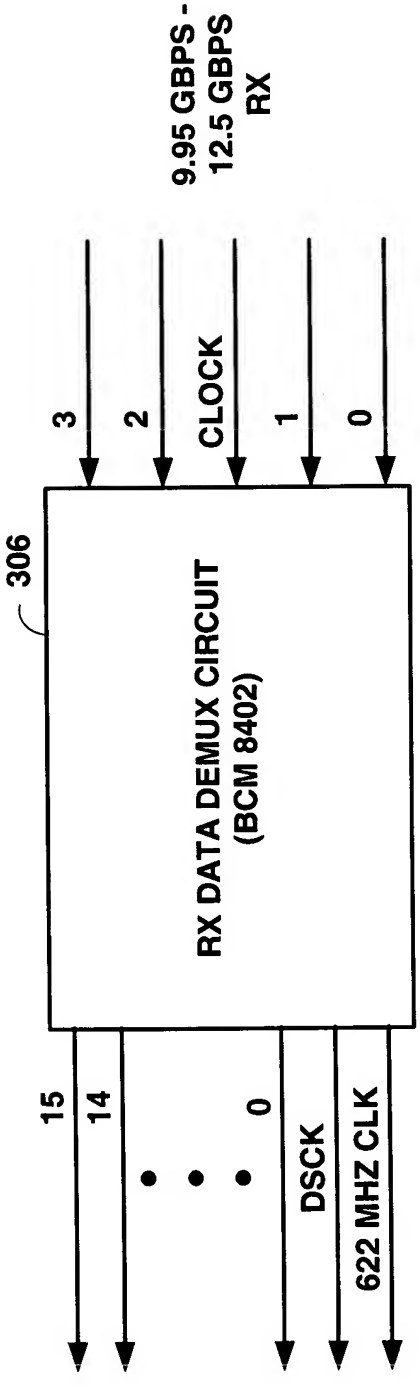

306
RX DATA DEMUX CIRCUIT
(BCM 8402)
15
14
0
DSCK
622 MHZ CLK
2.5 GBPS - 3.125 GBPS RX
3
2
CLOCK
1
0
9.95 GBPS - 12.5 GBPS RX

FIG. 4B

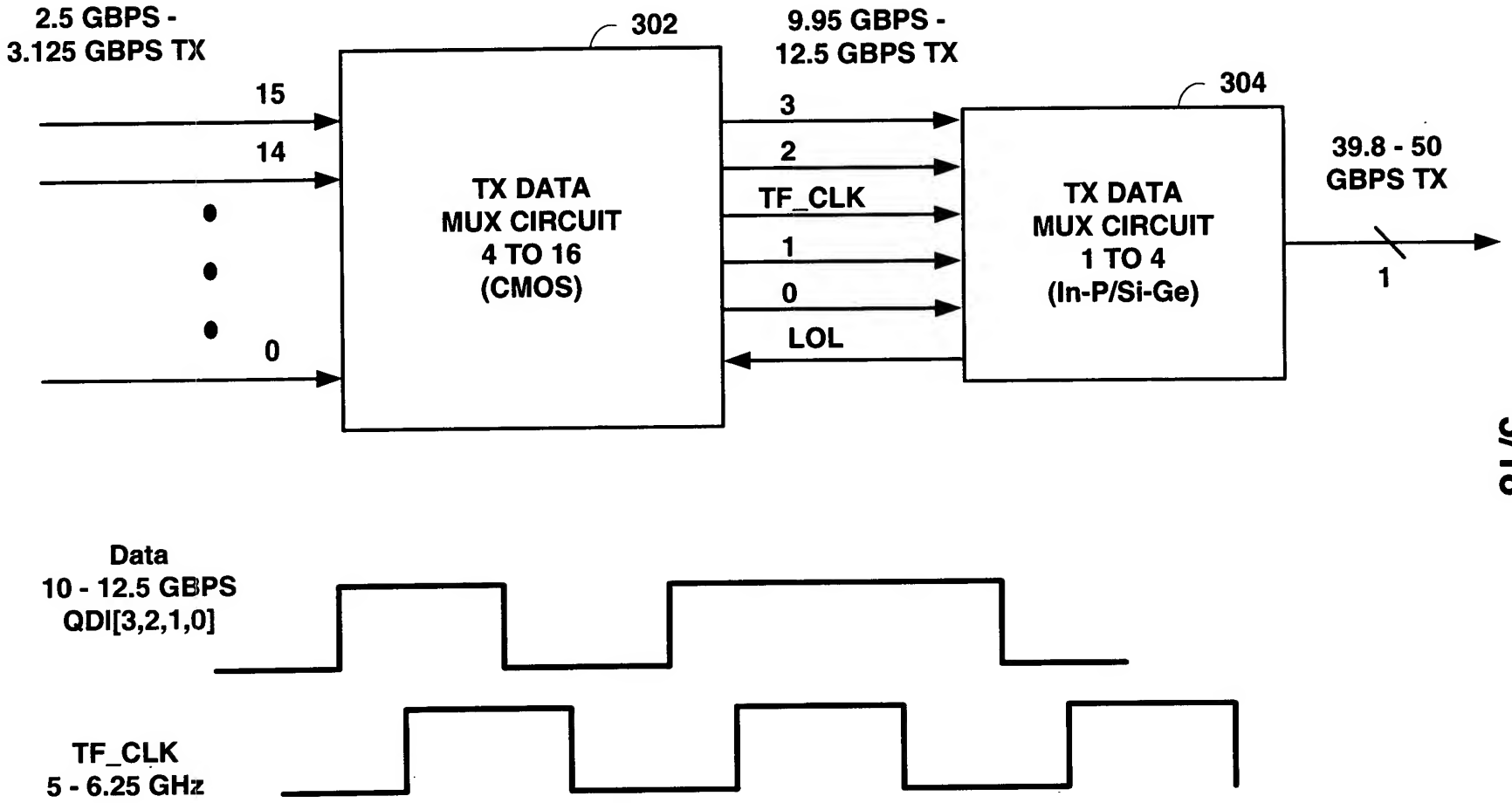

2.5 GBPS -
3.125 GBPS TX
15
14
0
302
TX DATA
MUX CIRCUIT
4 TO 16
(CMOS)
9.95 GBPS -
12.5 GBPS TX
3
2
TF_CLK
1
0
LOL
304
TX DATA
MUX CIRCUIT
1 TO 4
(In-P/Si-Ge)
39.8 - 50
GBPS TX
1
Data
10 - 12.5 GBPS
QDI[3,2,1,0]
TF_CLK
5 - 6.25 GHz

FIG. 5

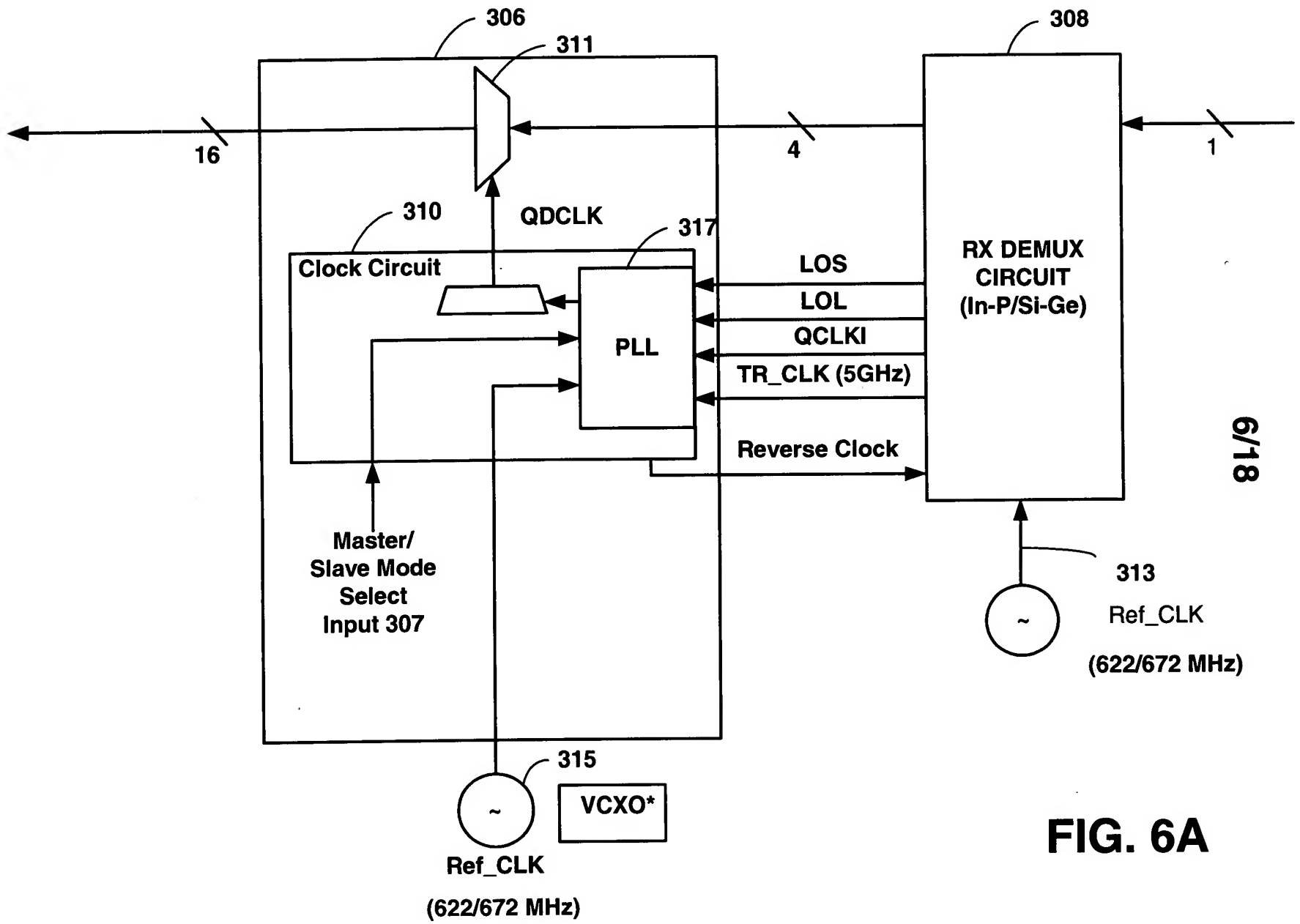

306
311
308
16
4
1
310
QDCLK
317
Clock Circuit
LOS
LOL
QCLKI
TR_CLK (5GHz)
PLL
RX DEMUX
CIRCUIT
(In-P/Si-Ge)
Reverse Clock
Master/
Slave Mode
Select
Input 307
313
Ref_CLK
(622/672 MHz)
315
VCXO*
Ref_CLK
(622/672 MHz)

FIG. 6A

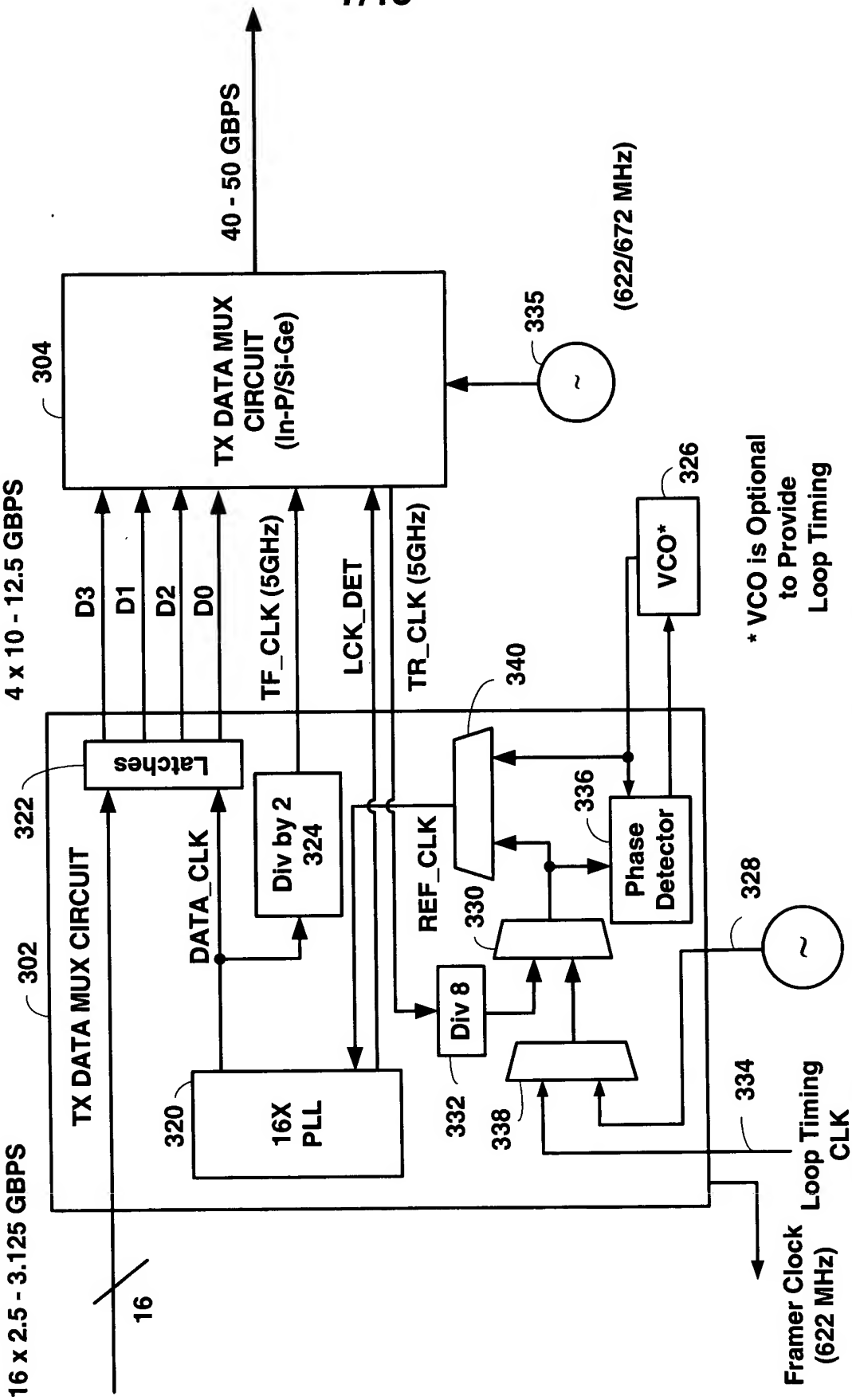

16 x 2.5 - 3.125 GBPS
16
TX DATA MUX CIRCUIT
302
322
Latches
320
16X PLL
DATA_CLK
Div by 2 324
4 x 10 - 12.5 GBPS
D3
D1
D2
D0
TF_CLK (5GHz)
LCK_DET
TR_CLK (5GHz)
304
TX DATA MUX CIRCUIT (In-P/Si-Ge)
40 - 50 GBPS
335
(622/672 MHz)
340
REF_CLK
330
Div 8
332
338
336
Phase Detector
326
VCO*
* VCO is Optional to Provide Loop Timing
328
334
Loop Timing CLK (622 MHz)
(622/672 MHz)
Framer Clock (622 MHz)

FIG. 6B

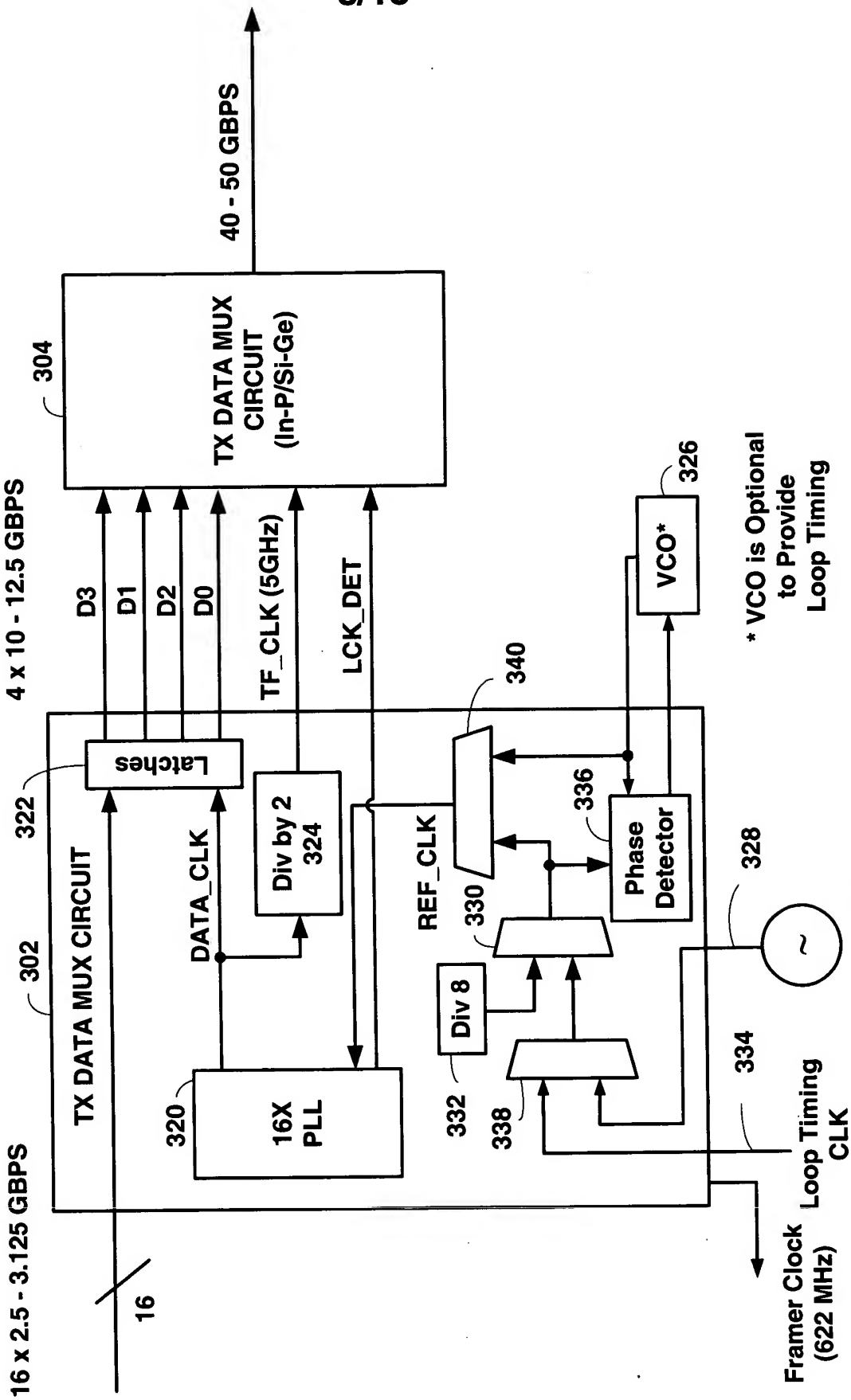

40 - 50 GBPS
304
TX DATA MUX CIRCUIT (In-P/Si-Ge)
4 x 10 - 12.5 GBPS
D3
D1
D2
D0
TF_CLK (5GHz)
LCK_DET
326
VCO*
* VCO is Optional to Provide Loop Timing
340
322
Latches
336
Phase Detector
328
DATA_CLK
Div by 2 324
REF_CLK
330
302
TX DATA MUX CIRCUIT
Div 8
320
16X PLL
332
338
334
16 x 2.5 - 3.125 GBPS
16
Framer Clock (622 MHz)
Loop Timing CLK (622 MHz)
(622/672 MHz)

FIG. 6C

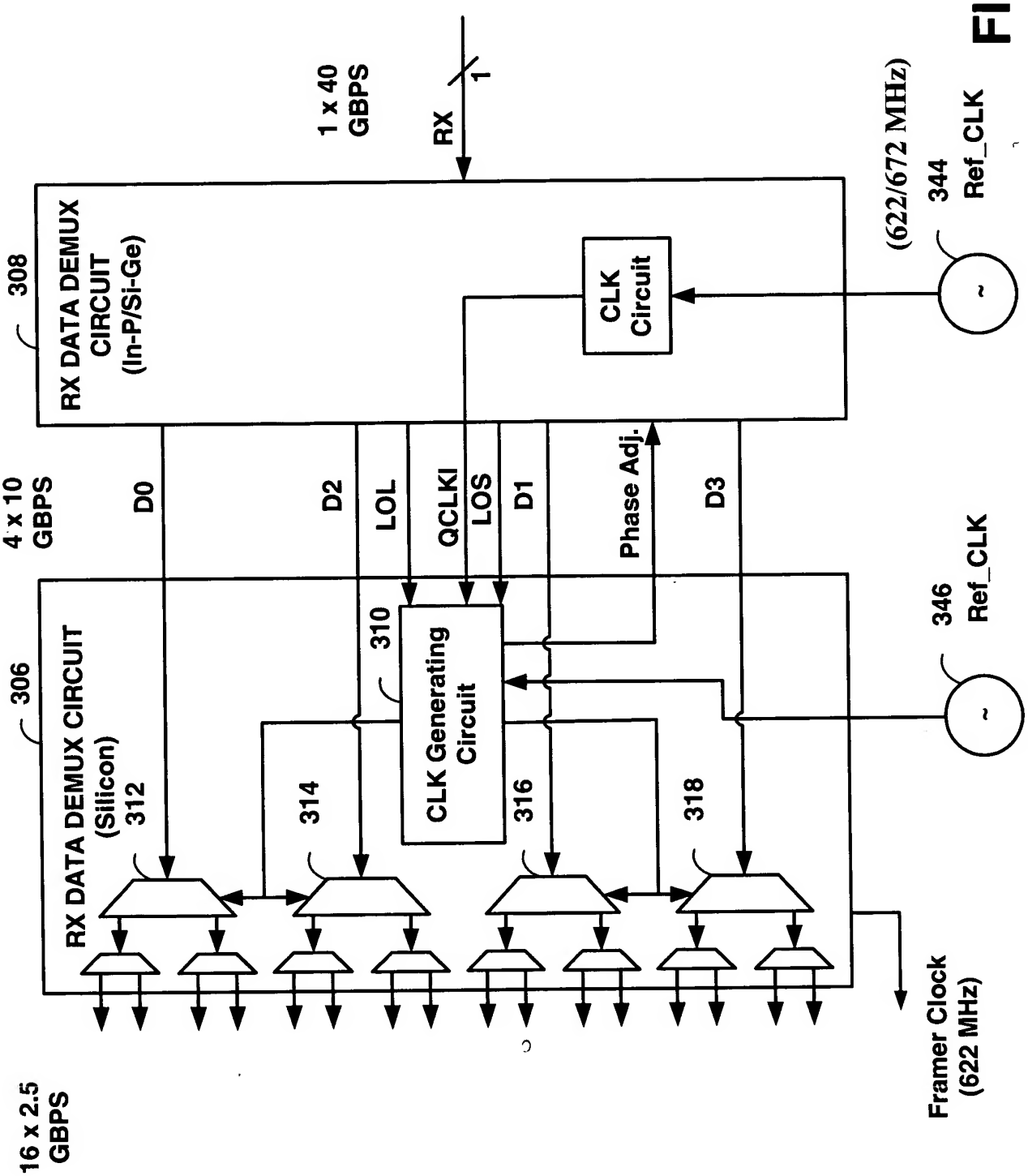

1 x 40 GBPS
RX
1
308
RX DATA DEMUX CIRCUIT (In-P/Si-Ge)
CLK Circuit
(622/672 MHz)
344
Ref_CLK
4 x 10 GBPS
D0
D2
LOL
QCLKI
LOS
D1
Phase Adj.
D3
306
RX DATA DEMUX CIRCUIT (Silicon)
312
310
CLK Generating Circuit
314
316
318
346
Ref_CLK
16 x 2.5 GBPS
Framer Clock (622 MHz)

FIG. 7A

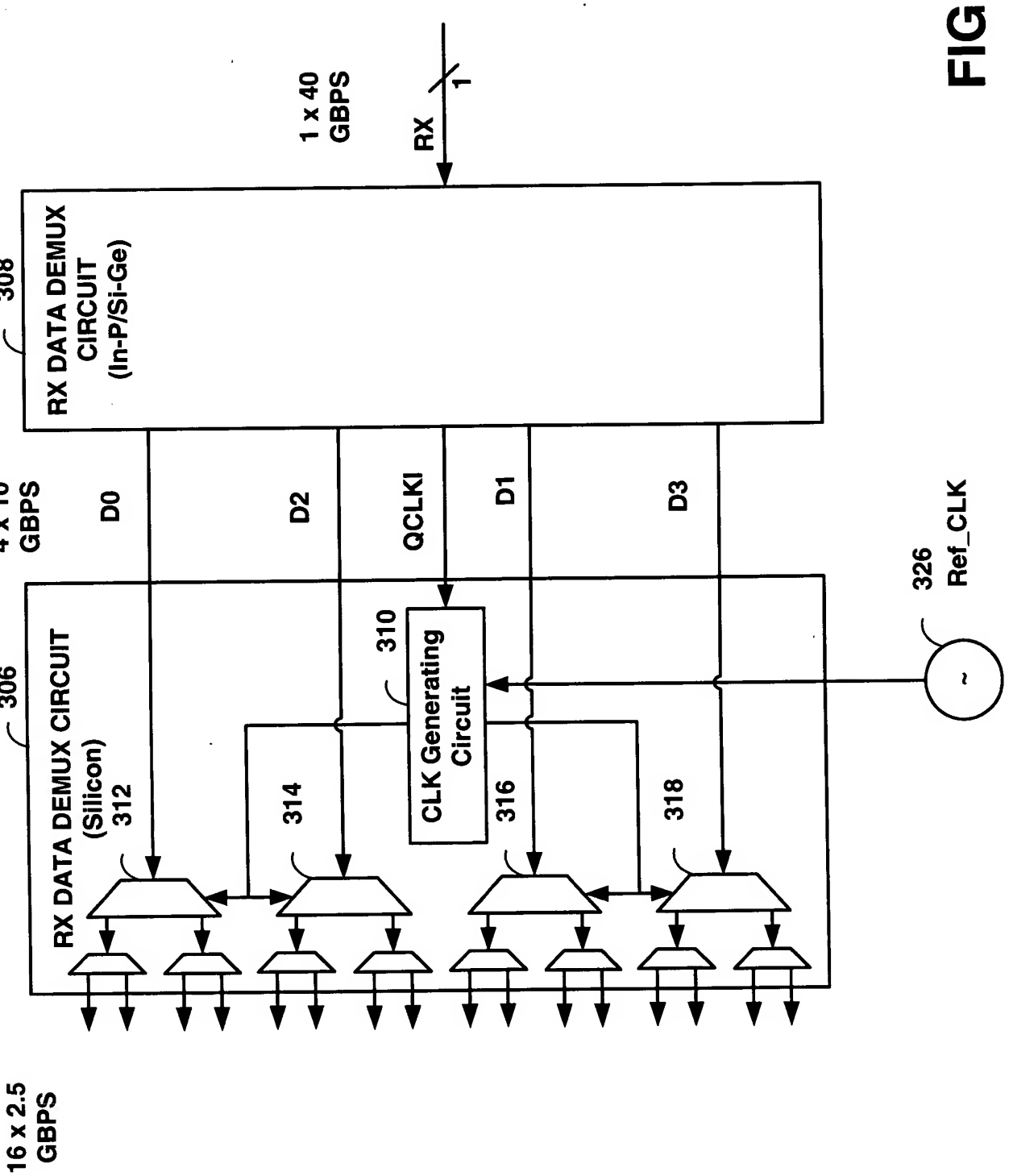

1 x 40 GBPS
RX
1
308
RX DATA DEMUX CIRCUIT (In-P/Si-Ge)
4 x 10 GBPS
D0
D2
QCLKI
D1
D3
326
Ref_CLK
306
RX DATA DEMUX CIRCUIT (Silicon)
312
310
CLK Generating Circuit
314
316
318
16 x 2.5 GBPS

FIG. 7B

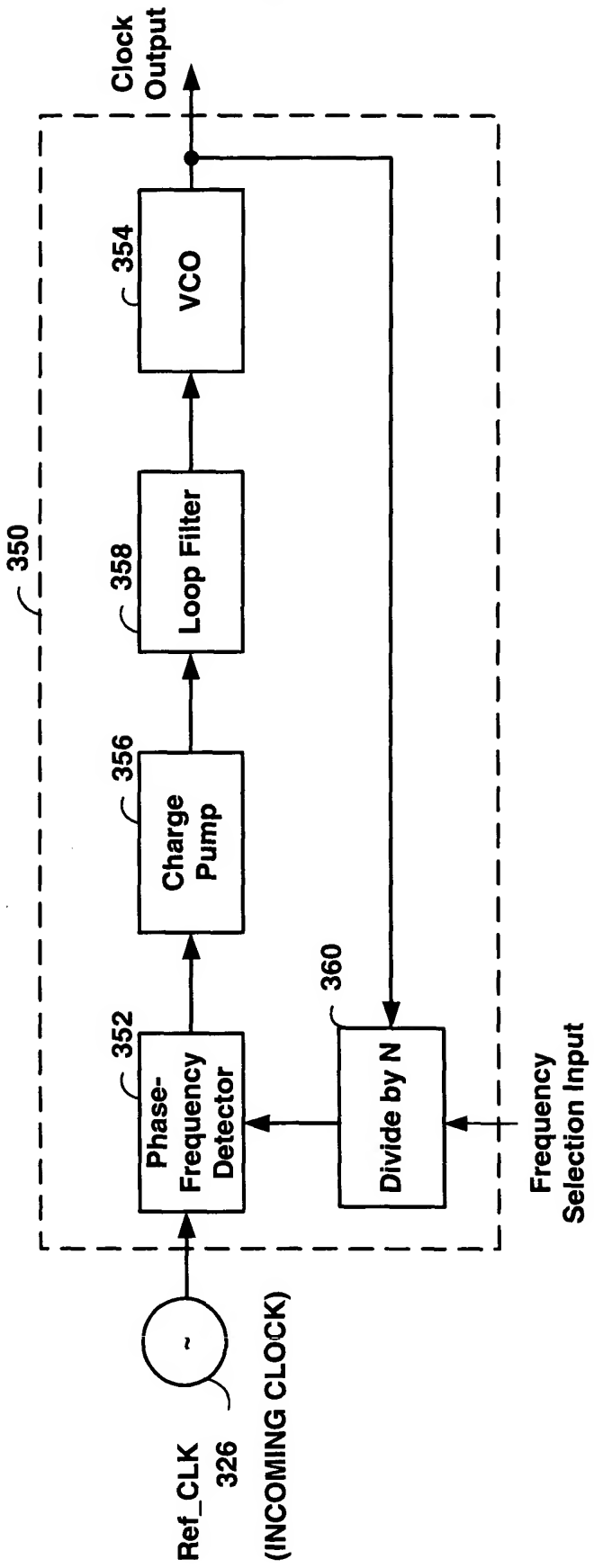

Clock Output
350
354
VCO
358
Loop Filter
356
Charge Pump
352
Phase-Frequency Detector
360
Divide by N
Frequency Selection Input
Ref_CLK
326
(INCOMING CLOCK)

FIG. 7C

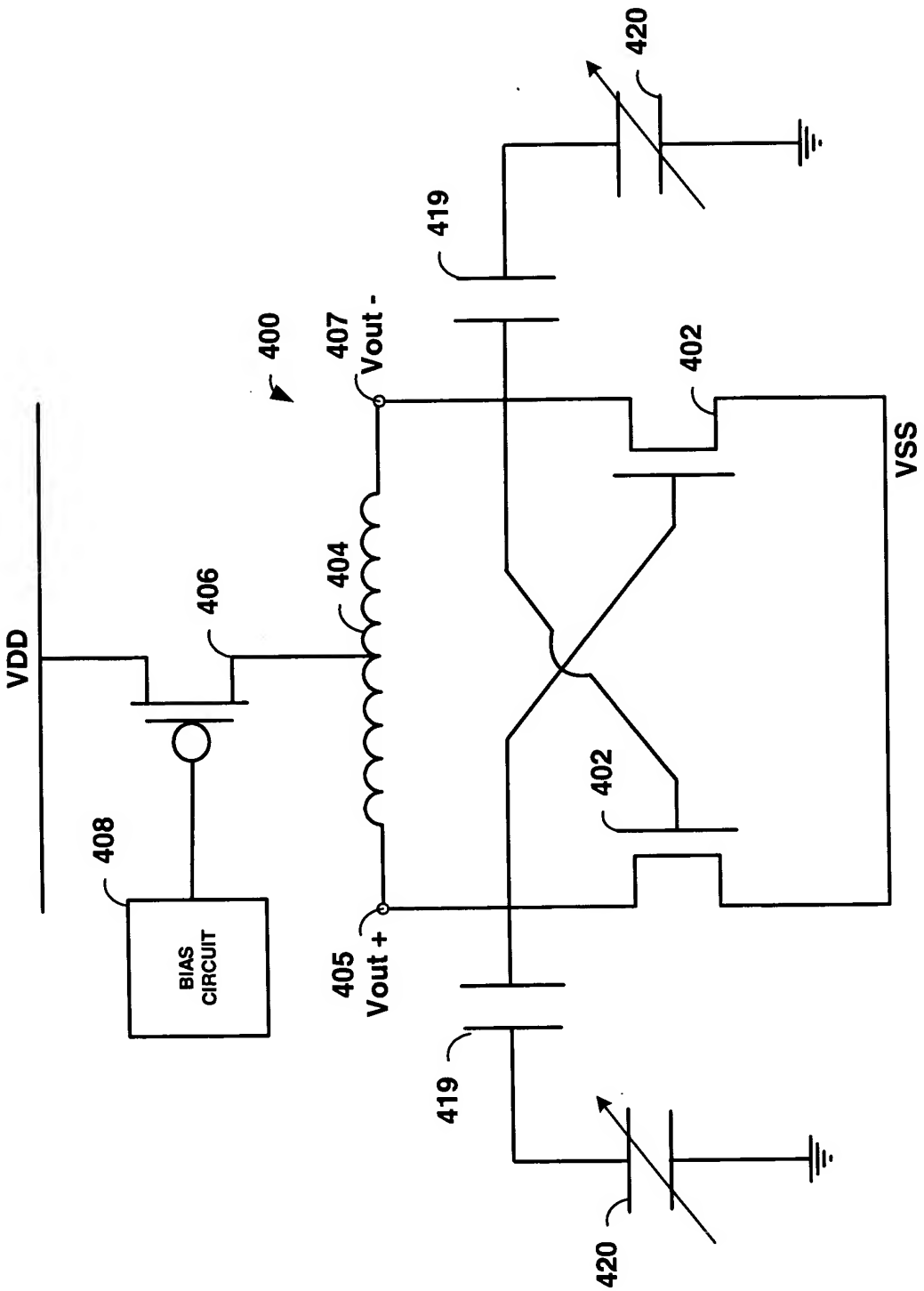

VDD
406
404
400
407
Vout -
405
Vout +
408
BIAS CIRCUIT
419
420
402
VSS

FIG. 8A

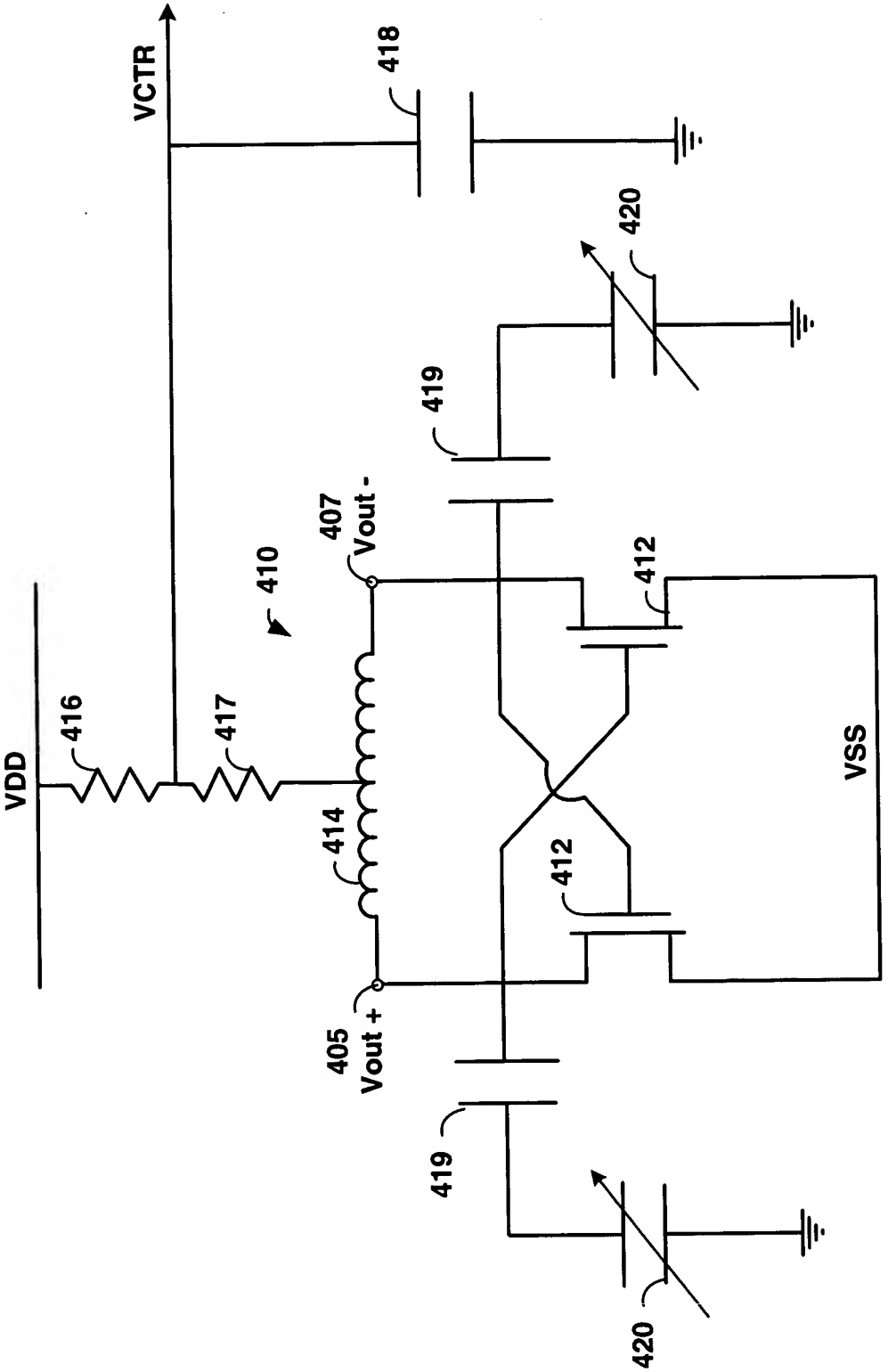

VCTR
418
420
419
407
Vout -
410
412
VDD
416
417
VSS
414
412
405
Vout +
419
420

FIG. 8B

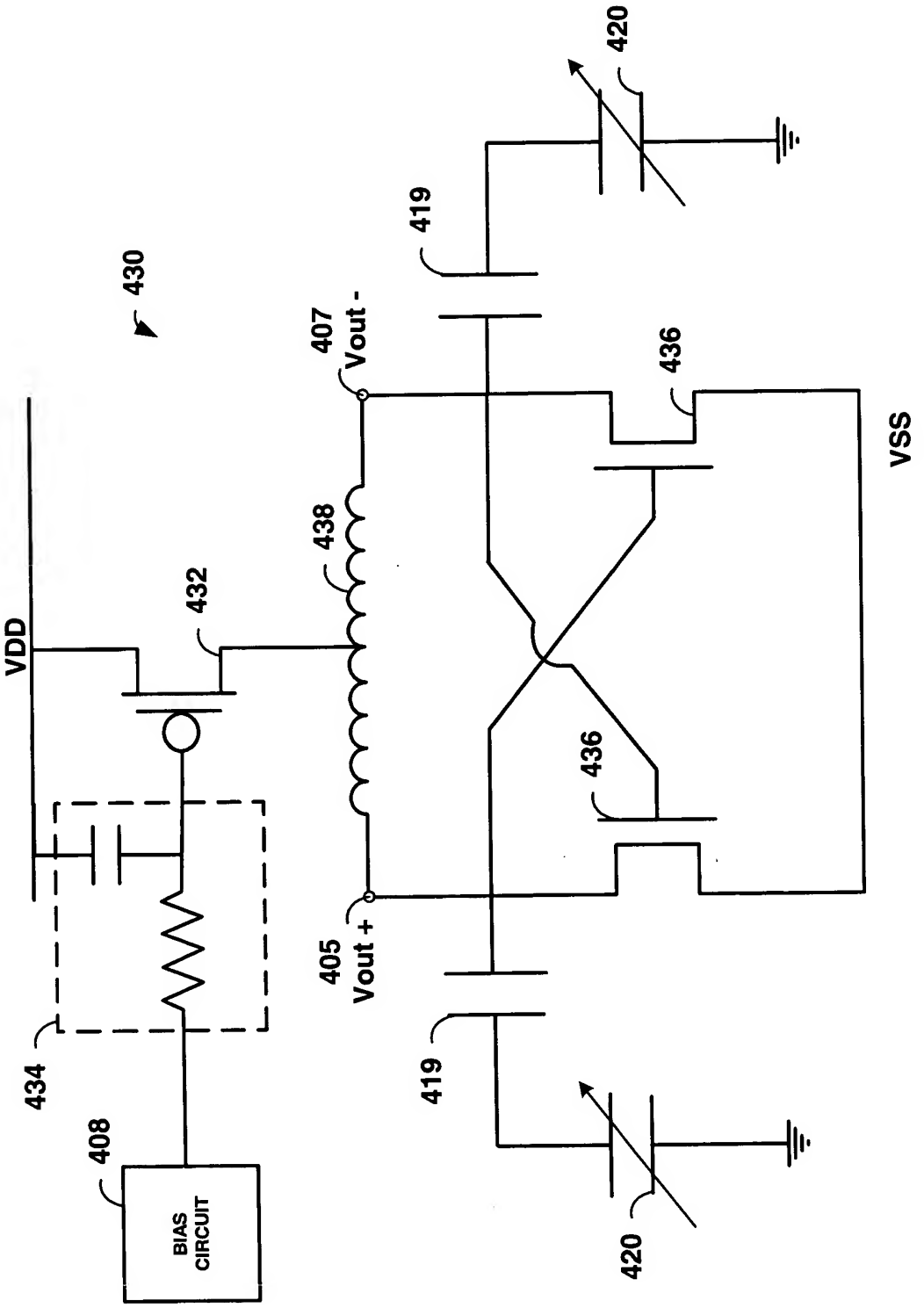

430
VDD
432
438
407
Vout -
405
Vout +
436
436
VSS
419
419
420
420
434
408
BIAS
CIRCUIT

FIG. 8C

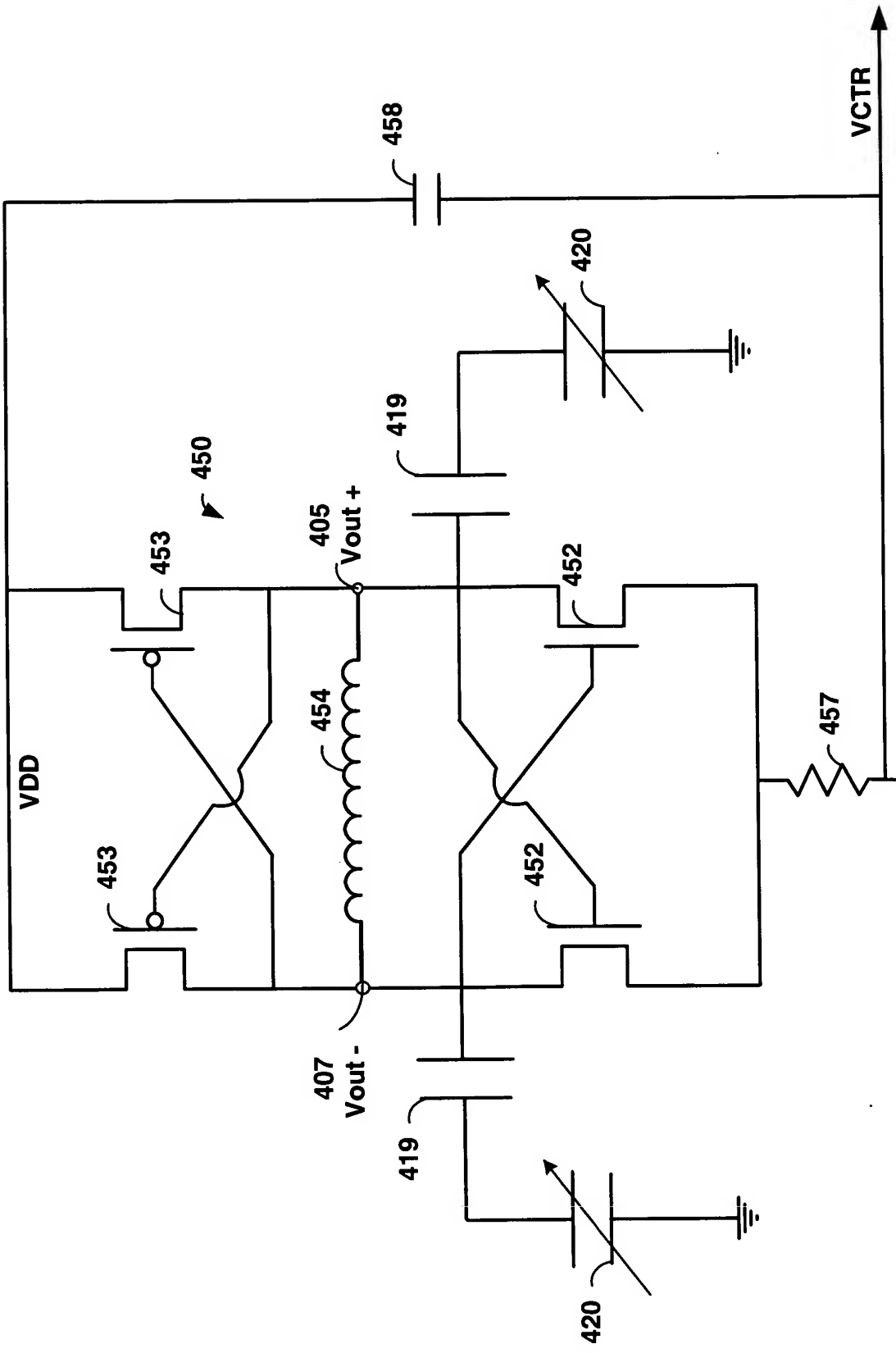
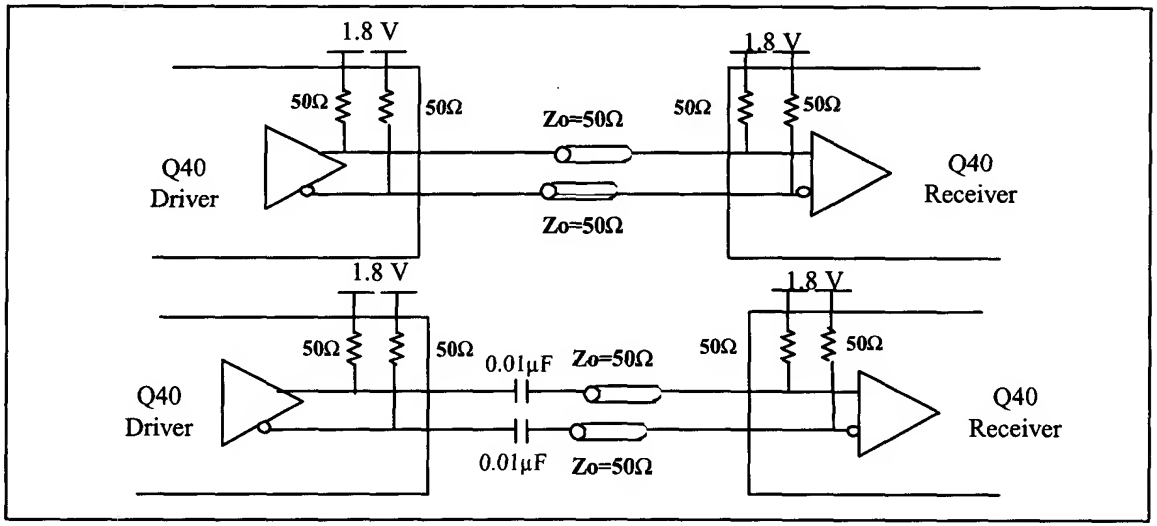

VCTR
458
420
419
450
405
Vout +
453
452
454
VDD
457
456
VSS
453
452
407
Vout -
419
420

FIG. 8D

Receiver Input and Source Centered Clock Performance

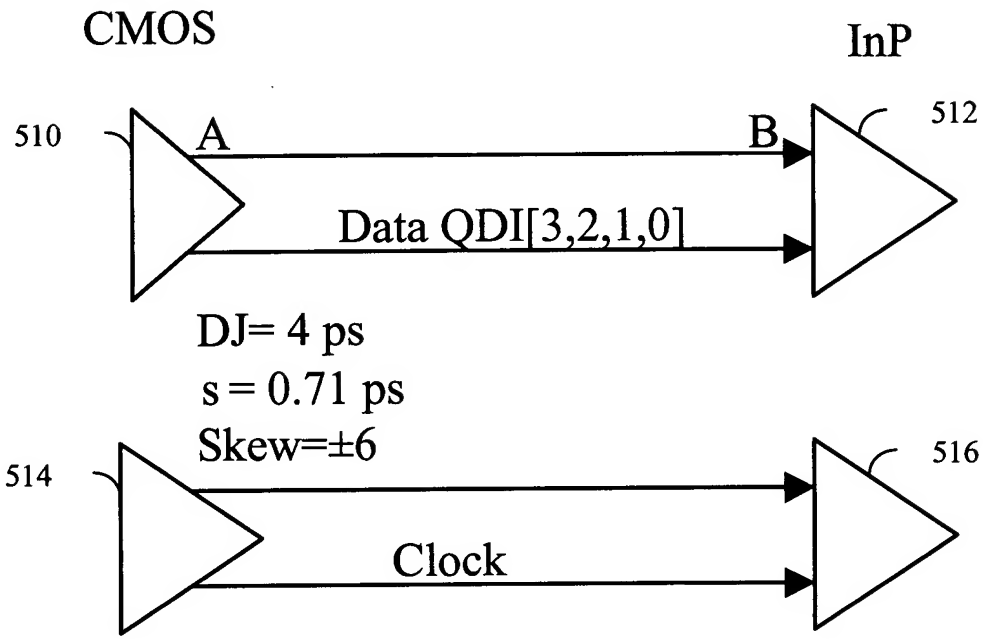
Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Output Common Mode	Vcm	See Figure Below	1575	1675	1775	mV
Single Ended Output Impedance	Z_{SE}		40	50	60	Ω
Differential Input impedance	Z_d		80	100	120	Ω
Input Impedance Mismatch	Z_M				10	%
Q40, CML Input Differential Amplitude, p-p	Δ VQDO	See Figure Below	400	500	600	mV
Q40 Input Rise and Fall Time (20% to 80%)	t_{RH} , t_{FH}			25	35	ps
Differential output return loss*	S11	Up to 7.5 GHz	10			dB
4-by-1 mux input return loss >15 db at 10 GHz						

500



502

FIG. 9



Additional Sources:
Crosstalk = 4 ps
PCB Mismatch = 4 ps

At B: Total Input Jitter = 4+4+12+4+4+4+0.71*14= 42 ps
CMOS Input Mismatch + setup/Hold = 24 ps
Margin at 10 Gig = 32 ps
Margin at 12.5 Gig = 12 ps

FIG. 10

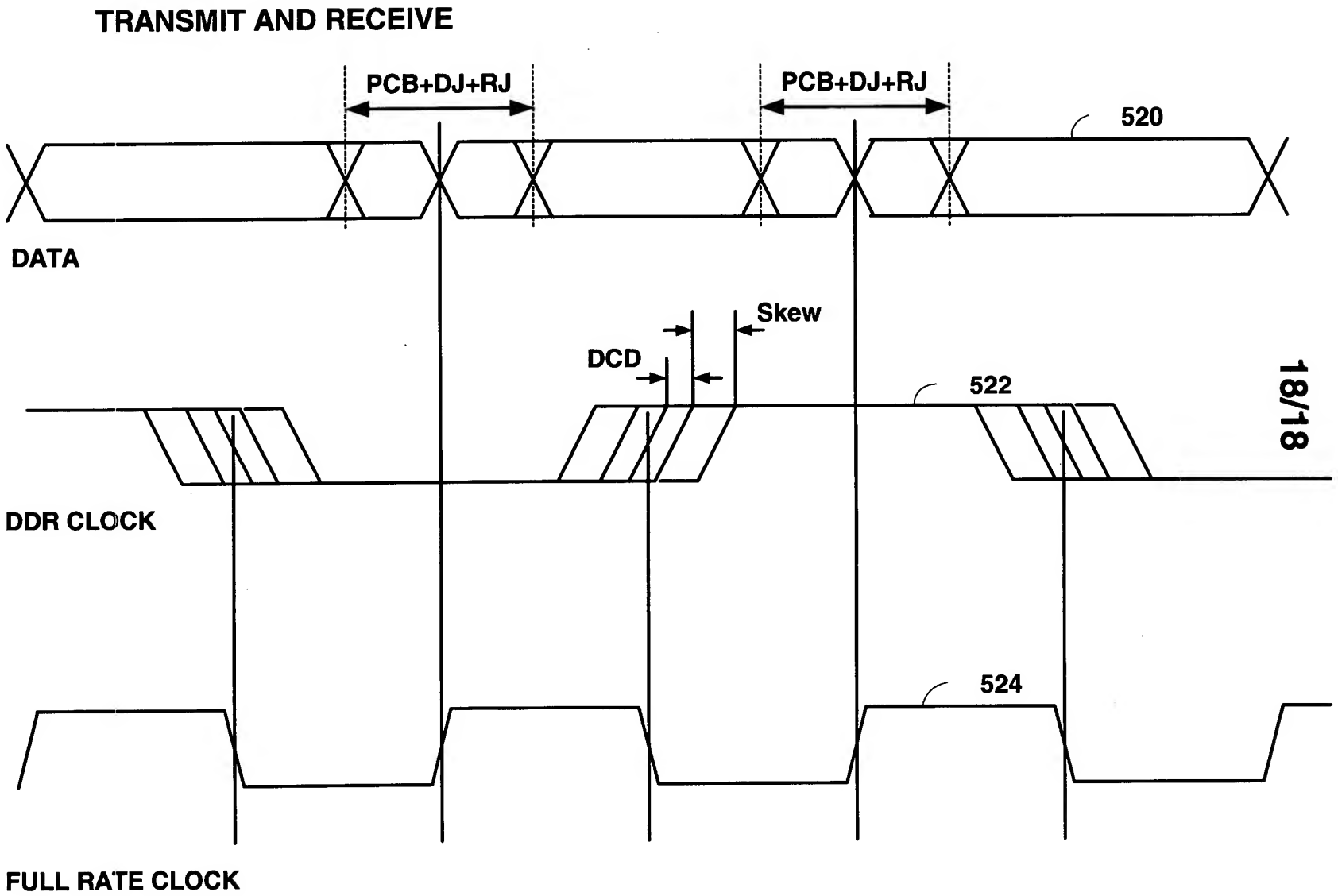

TRANSMIT AND RECEIVE
PCB+DJ+RJ
PCB+DJ+RJ
520
DATA
Skew
DCD
522
DDR CLOCK
524
FULL RATE CLOCK

FIG. 11